

OPTICAL SIGNAL INTEGRITY AND INTERPOLATION SIGNAL PROCESSING IN WIDEBAND SNS DIGITAL ANTENNAS

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Abstract: Symmetrical Number System (SNS) digital antennas provide high resolution direct digitization of wideband signals with excellent in-band signal rejection characteristics. This paper describes a prototype SNS digital antenna that uses 3 reflective interferometers ($m_1 = 63$, $m_2 = 64$, $m_3 = 65$), 253 comparators, and a Field Programmable Gate Array (FPGA) device to achieve 14 bit accuracy. Optical signal integrity and interpolation signal processing results are evaluated experimentally.

Introduction: A block diagram of a 3 channel wideband SNS digital antenna is shown in Figure 1. For each channel, the received RF energy (picked up by the antenna) is passed through a Low Pass Filter (LPF) for anti-aliasing and then fed through a DC bias/attenuation circuit to a reflective Mach-Zehnder

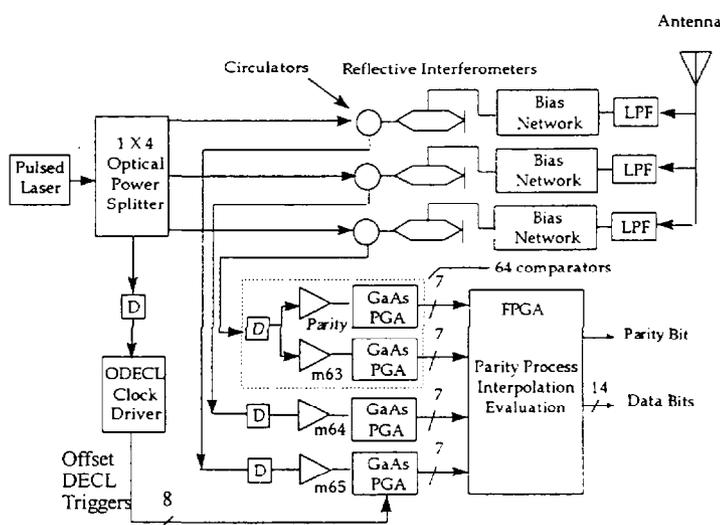


Figure 1. SNS digital antenna system block diagram.

interferometer (MZI). The optical input to the 3 interferometers is provided by a pulsed laser (6 ns pulse at a pulse repetition interval of 200 ns) that samples the RF signal. The optical pulse is sent through a 1X4 optical power splitter, through 3 circulators and on to the respective interferometers. The RF input signal applied to the interferometers modulates the amplitude of the laser pulse as a function of the interferometer's V_{π} . The laser pulse is then detected and applied to a DC restoration amplifier circuit and then amplitude analyzed by $m-1$ comparators where m is the channel modulus. The binary representation of the resulting comparator thermometer code for each channel is sent to a FPGA circuit for conversion to a 14-bit digital representation of the input analog signal. The timing of the digital encoding is controlled by an Offset Differential Emitter Coupled Logic (ODECL) adjustable trigger delay circuit. Note that the $m=63$ channel requires $2m = 126$ comparators that assist in correcting encoding errors that might occur [Ref. 1].

Optical Subsystem: The analog optical subsystem block diagram is shown in Figure 2.

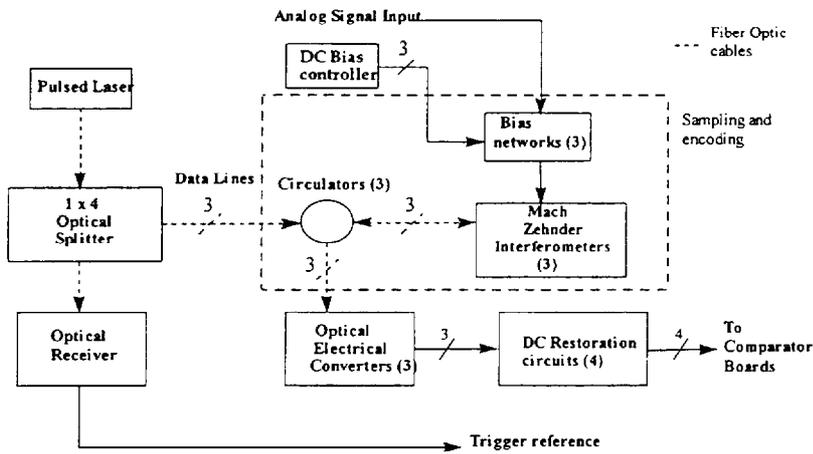


Figure 2: Optical subsystem block diagram.

Precise and efficient sampling is accomplished using a high speed semiconductor laser source which is triggered by a bit error encoder. The laser pulses are split off into four parallel signals, three of which are used to sample the RF signal while the fourth is used as a reference pulse for the ODECL adjustable trigger delay circuit that latches the output the comparator array. The analog RF signal to be sampled is fed

from the antenna and into the three bias termination networks. These networks distribute the input signal to the optical interferometers of the digital antenna and have adjustments for setting the moduli of the SNS and for phase shifting the interferometer transfer functions in order to align the folding waveforms across the three channels. The phase of the MZI folded waveform is a function of the DC voltage level on the electrode. Thus, DC bias on the electrodes provide a means to align the minimums of the parallel outputs in accordance with the SNS [Ref. 2]. The normalized output of the MZI is given by:

$$I(v, m) = \frac{1}{2} + \frac{1}{2} \cos \left(\frac{\pi}{m_i} v + \Delta\phi_i \right)$$

where the voltage dependent phase shift $\Delta\phi_i$ is used to phase the transfer function within each channel correctly. A passive termination network was also incorporated into the circuitry in order to provide a means of adjusting the MZI folding periods in accordance with the desired moduli ratios. Pulse amplitude modulation and SNS encoding is performed by three parallel, reflective MZI's. The laser sampling pulse is routed into the MZI via a circulator and modulated by the incoming RF signal in accordance with the linear Pockel's effect. The pulsed signal is encoded into the SNS and reflected back through the circulator and on to a detector/amplifier circuit.

Analog Opto-Electronic Conversion, Amplification, and DC Restoration:

The analog opto-electronic conversion process is shown in Figure 3.

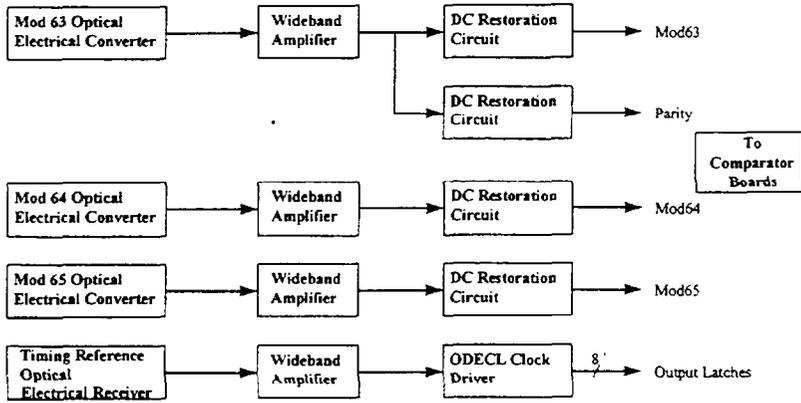


Figure 3: Analog opto-electronic conversion system block diagram.

comparator boards. An additional output is split from the Mod 63 channel in order to perform parity checking. Figure 4 shows the evolutionary process of our pulse recovery.

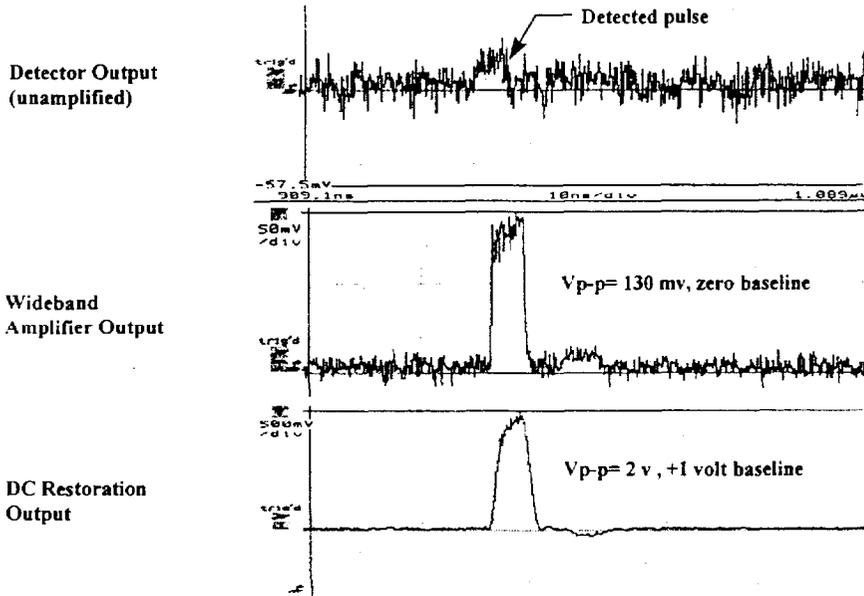


Figure 4: Detector output (unamplified), detector output (amplified), and DC restoration. The delay for all three channels is shown in Figure 5.

For each channel, the optical SNS encoded signal is detected (using germanium diodes) and amplified. The wideband amplifiers are ac coupled, dictating the need for a DC restoration circuit. This ensures that the signal is now operating between +1 and +3 volts DC, and away from the voltage rails of the

comparator boards. Because of the different delays inherent in all three channels, the ODECL adjustable trigger delay circuit is required to ensure that the comparator latches are triggered synchronously with the arrival of the analog data. Typical delays experienced are between 60ns and 70 ns for the three individual channels.

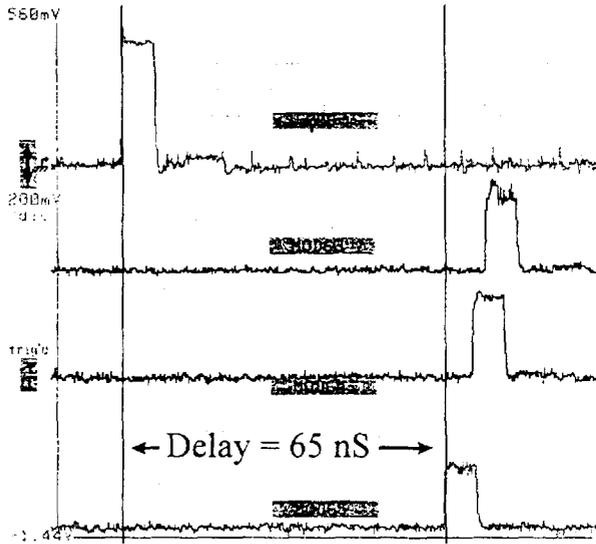


Figure 5: Mod-65, Mod-64, Mod-63, laser source output pulses at detector/amplifier

The ODECL adjustable trigger delay circuit reads the source pulse and triggers a delayed differential emitter coupled logic pulse that latches the comparator outputs when the data is valid. A block diagram of the adjustable trigger delay circuit is shown in Figure 6.

A comparison of a 500 kHz triangle wave (antenna input signal) and the modulated, SNS encoded analog pulse is shown in Figure 7. From this figure we can see that the maximum values of encoded output correspond to one folding period.

The sampled input signal in each channel (SNS encoded pulse) is now ready to be amplitude analyzed by the m-1 comparators.

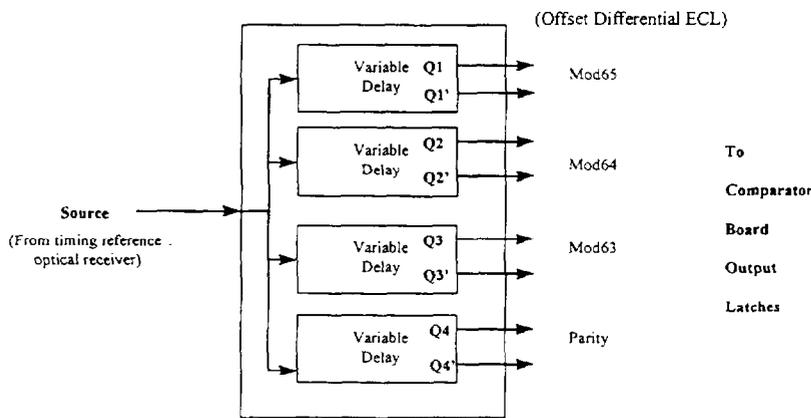
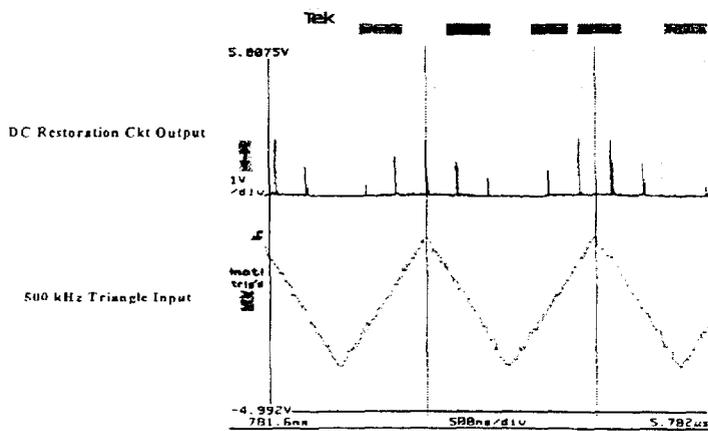


Figure 6: Adjustable ODECL trigger delay circuit block diagram

Digital signal conversion and processing:

A block diagram of the GaAs comparator circuitry is shown in Figure 8. Each comparator board consists of eight Maxim (MAX547) 13 bit digital-to-analog converters which control the 64 matching reference voltages to the comparator array. Each chip consists of 64 comparators which turn on when the matching reference voltage is exceeded. We note that the distribution of the matching reference voltage is non-linear [Ref. 2]. The thermometer code is then latched by the trigger from the ODECL trigger delay circuit described above. This ensures stability of the output over the next trigger period (for our purposes, 200ns). The thermometer code is then converted to a seven bit digital representation.



* Voltage applied equivalent to one V_{T1}

Figure 7: Folded output versus analog input voltage

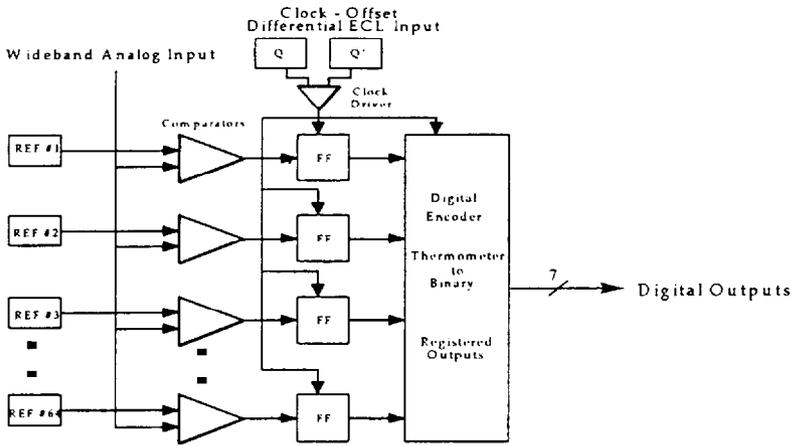


Figure 8: Comparator circuitry block diagram. (SPEC).

than 14 bits. Only 2^{14} levels are utilized because a maximum of only 130 folds are available from the interferometers.

Parity Processing:

In order for the Optimum SNS system to decode the input magnitude of the signal properly the comparators for the different moduli (channels) have to switch at the same instant. This is shown in Figure 9 which depicts the comparator encoding scheme for a simple two moduli ($m_1 = 4, m_2 = 5$) encoder. If the comparators do not switch exactly at each LSB transition, an encoding error will occur.

A fourth (parity) comparator circuit (m_1+1 comparators) has been established to provide an indication of whether or not the sample has occurred within a region where a slight offset of the comparator alignment may occur. This is accomplished by the creation of parity bands. Using the smallest modulus m_1-1 comparators and the parity comparators, parity bands can be established around the code transition points. If a sample occurs within one of the parity bands

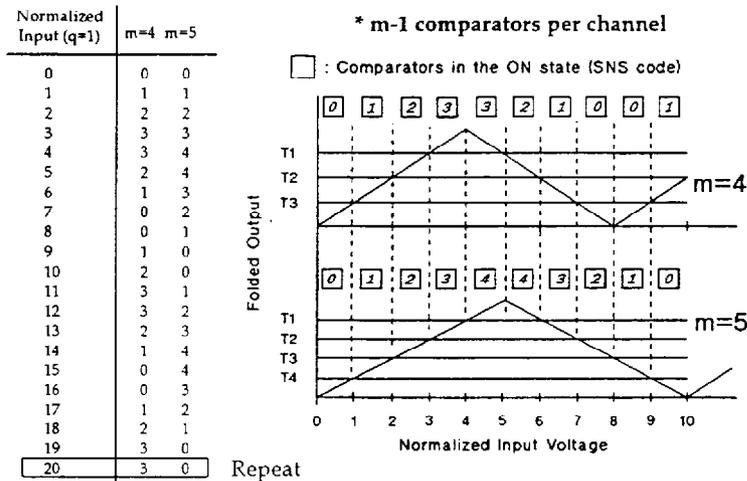


Figure 9: Comparator encoding scheme for moduli 4,5 encoder.

comparators (odd parity) indicates the sample is good.

High resolution is obtained when the three parallel SNS outputs are recombined. The dynamic range M of an N-channel SNS system is

$$M = \prod_{i=1}^N m_i$$

which for this system,

$$M = 63 * 64 * 65 \Rightarrow 262080 \text{ levels.}$$

This is considerably more

the signal may be unusable and interpolation processing will be performed on that sample. The parity encoding scheme for the simple modulus 4 and 5 encoder is shown in Figure 10.

Determination of whether the sample has occurred within a parity band is made using a simple exclusive-or logic comparison to verify the number of comparators in the mod63 and parity channels turned on. An even number of comparators is considered even parity and the sample is possibly bad. An odd number of

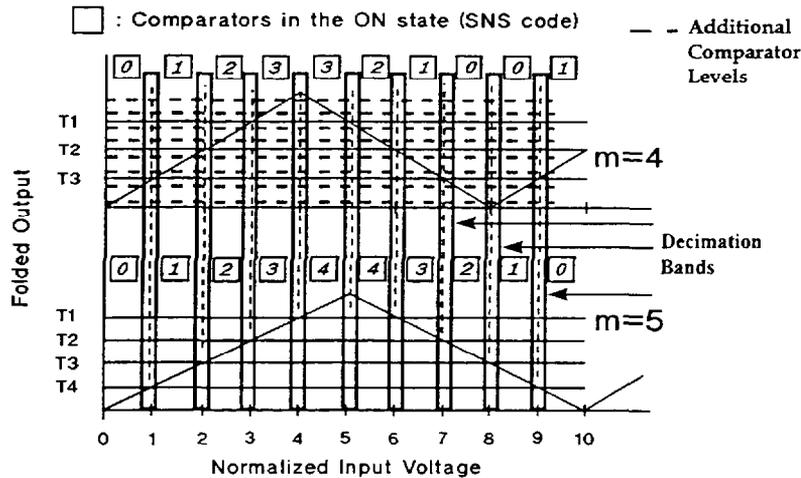


Figure 10: Parity processing scheme for moduli 4 & 5 SNS encoder.

with a recent study that has shown the most efficient parity processing algorithm is to replace the possibly bad sample with the last received good one [Ref. 4].

The conversion from SNS to binary is carried out in three steps; conversion from SNS residues to RNS residues, conversion from RNS residues to 18 bit binary representation based on RNS, and finally a conversion to an 18 bit binary representation of the input applied voltage. Due to the limitation of the number of folds possible with the present interferometers only 14 bits of the final output are used. The process is designed using a Xilinx XC4003E FPGA and Xact Step 6 software interfaced using Foundation Active Cad. A schematic representation of the design is shown in figure 11.

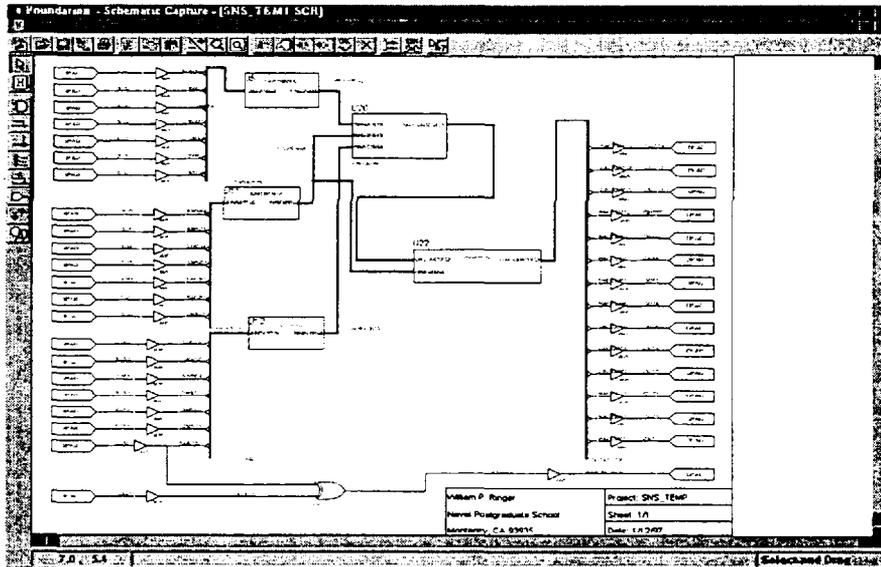


Figure 11: SNS to digital FPGA design.

References:

- [1] P. E. Pace, J. L. Schafer, and D. Styer, "Optimum analog preprocessing for folding ADC's", *IEEE Trans. Circuits Syst. II*, vol. 42, pp.825-829, December 1995.
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- [3] P. E. Pace, D. Styer, and W. P. Ringer, "Optimum SNS to binary conversion", *IEEE Trans. Circuits Syst. II*, to be submitted.
- [4] Byeong-Jun Park, "Interpolation techniques in high resolution residue antenna architectures" *Master's Thesis, Naval Postgraduate School, Monterey, CA*. September 1996.