

DATA ACQUISITION SYSTEM FOR COMPUTER

AIDED COHERENT ACOUSTIC IMAGING

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ABSTRACT

A coherent acoustical imaging is under design and test. This system utilizes precisely spaced samples of the amplitude and phase of an ultrasonic field as data input for the computer processing and display sub-system. Two designs of the data acquisition system are described: one a raster scan and the other a single sweep of a linear array. Design goals are to achieve a 256 x 256 array of amplitude and phase data recorded on a digital cassette recorder. Both techniques use microprocessor control of the data flow and sampling. The relatively slow motion of the raster scan presents few problems in achieving results and control was easily implemented with an 8748 microprocessor. The speed requirement in sampling, measuring and converting the data in the linear array case however present a more difficult challenge requiring a more complex microprocessor system described in detail in the paper.

INTRODUCTION

The imaging system^[1] under study consists of a computer that can perform backward wave propagation and other image processing operations on coherent ultrasonic data. The computer generated image is displayed on graphical output devices in an interactive fashion. The data acquisition portion of the system, the subject of this paper, needs to provide a square array of data samples that measure the amplitude and phase of the ultrasonic field in question. Data field sizes are operator controlled with repre-

sentative sizes being 64 x 64, 128 x 128, and 256 x 256. Sample spacing is controlled by a precision scanner with a usual sample spacing of .75 mm (one-half wavelength at the 1 MHz operating frequency). Scan geometries, speed and automatic operation are controlled by limit switches and a hardware controller. One option for the future is to bring this portion of the system also under microprocessor control.

Currently two modes of scan geometry are under active investigation. The first is a comparatively slow raster scan over the data field by a single point receiver. This scan is useful with static objects for the production of data to be used in the study of processing options and interactive techniques on the computer side of the system. The second scan is a single sweep of a large linear array with high speed sampling and multiplexing of the data columns producing the square data array. Other scan geometries are also easily implemented in this system; in fact, one of the primary advantages of a computer based system is the flexibility of the technique to investigating novel geometries and/or processing options.

Microprocessors help to achieve additional flexibility in the data acquisition system. In the present system the devices control the data flow through the digitizers, synchronize the electronic hardware and control the recording devices. The addition of moderate memory capacity allows for full buffering of the data before recording and/or transmission to the computer. While current microcomputer systems do not have speed or data handling capability required for a true stand-alone imaging system, rapid rate of improvement and predicted performance levels holds the promise of small inexpensive imaging systems based on microcomputers vs the present-day minicomputer systems.

SYSTEM FOR RASTER SCAN

The goals of the system^[2] designed to work with the slow speed raster scan include control of data flow (Fig. 1) from the A/D converters to the recording devices, data conversion, between binary, BCD and ASCII formats, and interfacing to the various peripheral devices. To illustrate the requirements the following features of various peripheral devices are listed:

Line printer--This device has an 'RS-232-like' interface (hence allowing the interface to also be used for CRT or video displays) that requires ASCII characters to be transmitted at a 2400 baud rate with a proper parity bit and two stop bits inserted after the seven data bits.

Teletype terminal--This device requires a 25 ma current loop drive with ASCII data at a 110 baud rate. Again proper parity bits must be inserted into the data stream. (The Teletype paper tape capability has also provided a backup recording capability to the cassette recorder.)

Digital cassette recorder--This device, providing 2.2 megabits of storage requires straight binary data at CMOS voltage levels at a rate of 23 bits/sec. Start/stop signals and read/write controls must also be provided since the recorder operates only when data is present.

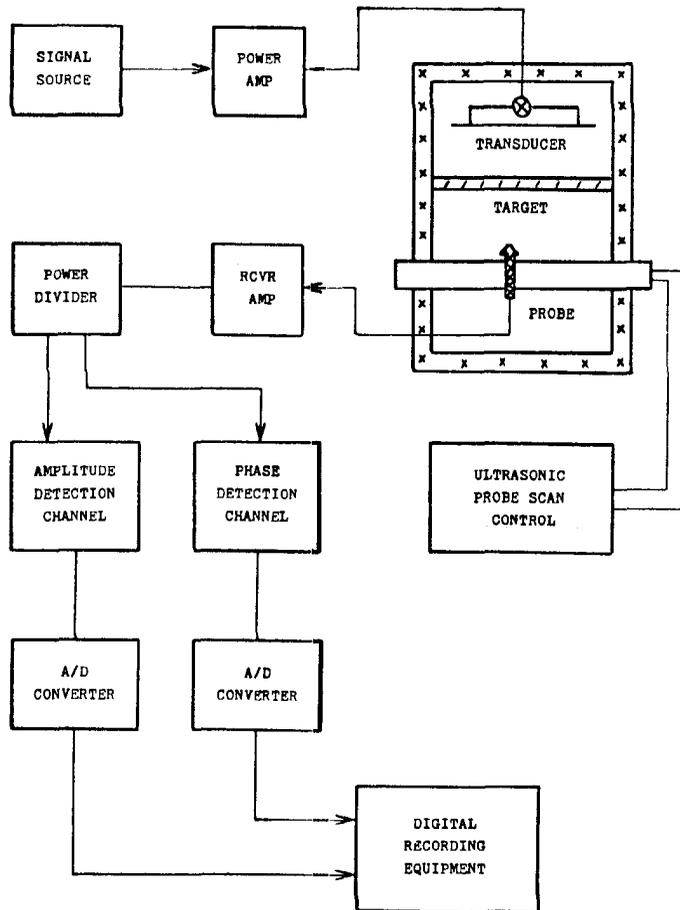


Figure 1. System block diagram

The system implementation was based on an Intel 8748 micro-computer with various output drivers, an I/O address decoder and status displays. The system was programmed and debugged using an Intel PROMPT 48 development system in an emulate mode to simulate the microprocessor with the actual I/O hardware connected to the development system extender card. The software structure, chosen for enhanced flexibility, uses an executive program under operator control through a touch pad keyboard to call the appropriate sub-routines. The subroutines are performed as triggered by the sample signal generated by the raster scan equipment.

As an example, consider the case where one wishes to write the data on the Teletype unit (and punch a paper tape). The operator presses the keys for the Teletype program and begins the scan process. The analog values of the amplitude and phase are sensed continuously and fed to the A/D converters. At the sample signal the A/D converters sample and hold the values and perform the A/D conversion. The microprocessor is also triggered by the sample pulse and waits for the end-of-conversion signal from the A/D units (a nominal 4 μ sec.) When the pulse is received, the microprocessor reads the data from the amplitude A/D unit on its I/O ports, converts the binary data to BCD for internal manipulation, converts the BCD data to ASCII, adds a start baud, two stop bauds and a parity baud as required by the Teletype, and presents the data stream to the proper I/O port by use of the current loop driven to the Teletype. The process is then repeated for the phase data before the next sample. Sampling time is limited to 1 sample/sec by the response time of the Teletype (especially the carriage return and line feed mechanics).

Software reprogramming and additions are easily accommodated. In fact the Teletype unit was added to the system at a late date due to a failure of the cassette recorder mechanism. The microprocessor was easily reprogrammed, debugged and the unit was quickly added to the system once the TTL to 25 ma current loop adapter was designed and implemented. Additional testing and calibration options have been included throughout the software to test the various hardware elements and data manipulations in the system.

SINGLE SCAN LINEAR ARRAY SAMPLING^[3]

A single lateral scan of a linear array can produce the data matrix in time of a single row scan. The requirement for a rapid-fire sampling of the column element requires comparatively fast processing electronics. If a 256 element is sampled every 500 milliseconds, for example, the sample interval is approximately 2

milliseconds. Faster sweep times reduce the sampling time accordingly. While these rates are not fast electronically much of the phase and amplitude sensing as well as the microprocessor control had to be redesigned to accommodate this speed. The sampling rate is also much higher than the recording rate or transmission rate of the peripherals necessitating the requirement for an electronic memory to buffer the data until ready for recording. Since 256 x 256 x 8 bit memories are needed for both the amplitude and phase, two 64K byte memories are required. Not available on the microprocessor chip with only a 1K RAM, a memory expansion capability was one system requirement. It should also be noted that only dummy data was tested since the large linear array will not be built until the raster scan technique has been thoroughly tested.

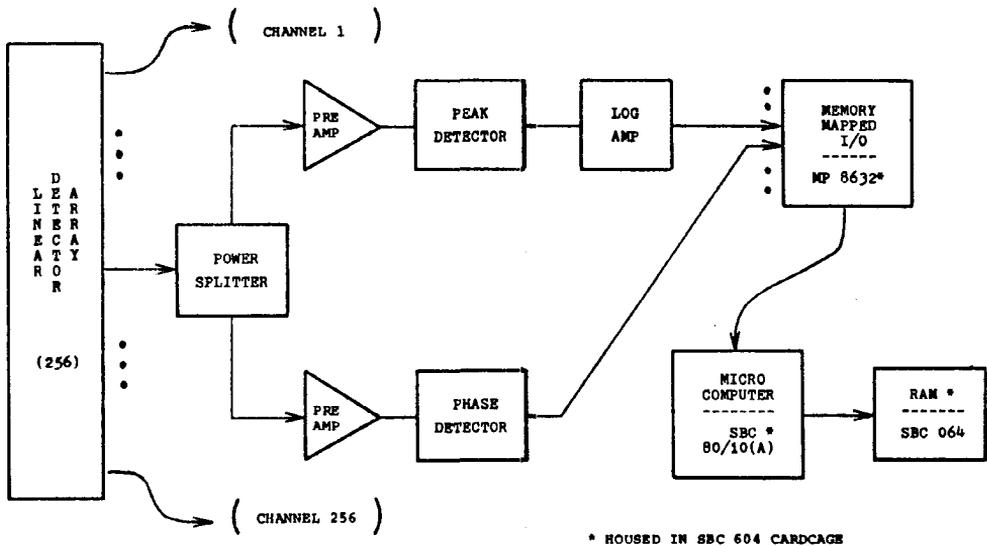
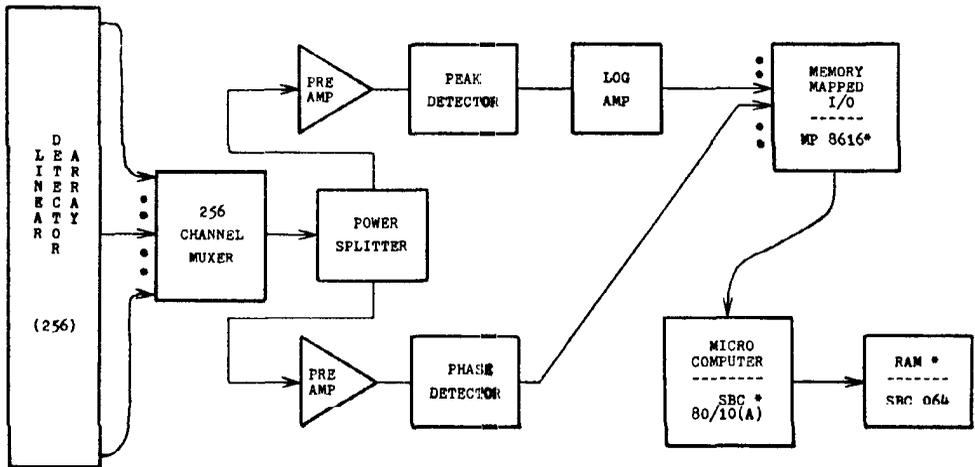


Figure 2. Block diagram of multichannel detector system

Two alternative systems were considered. The first (Fig. 2) required multiple amplitude and phase detectors whose output was multiplexed and read into memory by the microprocessor system. The second (Fig. 3) multiplexed the samples of the 1MHz signal onto a single channel which measured the amplitude and phase of the successive samples and read these into the microprocessor I/O ports for digitizing a memory assignment. A trade off study of the electronic costs show a 12:1 advantage for the latter system with a cost of only \$7,000.



* HOUSED IN SBC 604 CARD CAGE

Figure 3. Block diagram of multiplexed single detector system

As shown in Fig. 2 the primary elements of this system are the multiplexers, phase detector, amplitude detector and microprocessor system. Each of these will be described in some detail.

The primary component of the multiplexer is a sixteen channel CMOS switch. As shown in Fig. 4, 16 devices are cascaded to provide full coverage. An 8 bit counter successively enables each device and switches in the channels through an on-chip decoder. A seventeenth device multiplexes the output of the sixteen others. Primary considerations in checking the switching performance were switching transition time and crosstalk effects on the amplitude and phase transmission performance. Switching transition times were typically measured as $1\ \mu\text{sec}$ presenting no problem. Crosstalk effects are more complicated since both amplitude and phase can be affected. Changing adjacent channel amplitudes over a 60 dB range caused a worst case channel transmission change of 2.5 dB. Phase distortion was minimized by the choice of channel load levels. A $100\ \Omega$ load produced the least phase distortion (less than $.3^\circ$) but requires buffer amplifiers to interface with the A/D convertor. The ON channel attenuation was also maximized to $-10\ \text{dB}$ with this load but could be made up with the buffer amplifiers. This ON channel attenuation was also found to be signal dependent but a signal independent range ($\pm 2\ \text{dB}$) was found to exist for signal values between $-40\ \text{dBV}$ and $0\ \text{dBV}$. Larger dynamic ranges are possible by including a nonlinear correction in the computer processing but, lacking this refinement, the multi-

plexer restricts the system's dynamic range to 40 dB. (Other components have proven to have at least 50 dB dynamic range.)

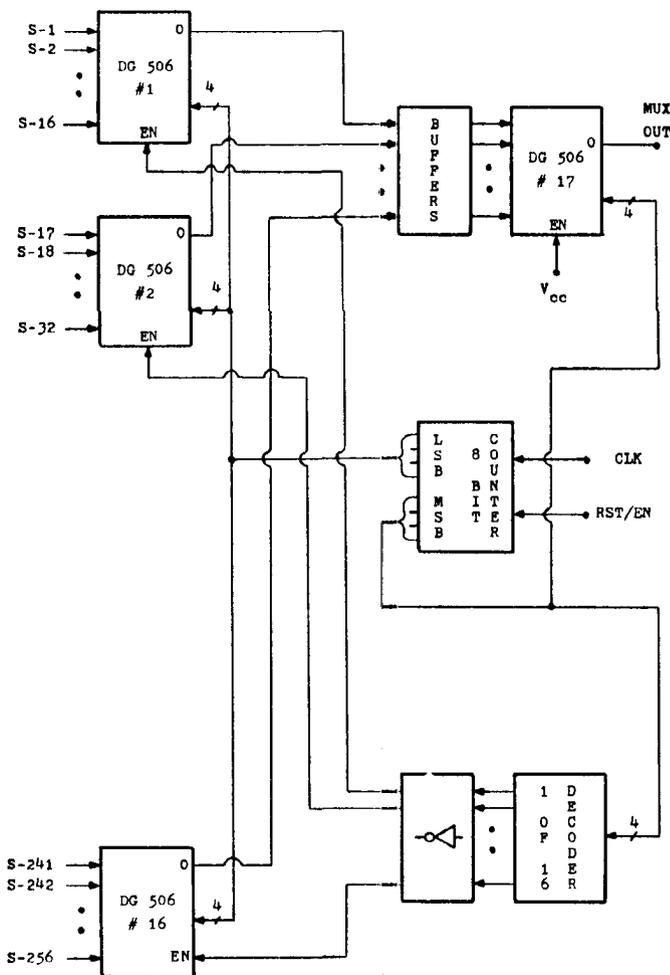


Figure 4. Multiplexer subsystem

The high speed phase detector circuit^[4] shown in Fig. 5 uses voltage comparators for limiting and digital logic for determining phase. Figure 6 shows the response (lower trace) of the phase detector circuit to the burst shown in the upper trace. A .2 msec delay is encountered which must be accounted for in triggering the A/D converters.

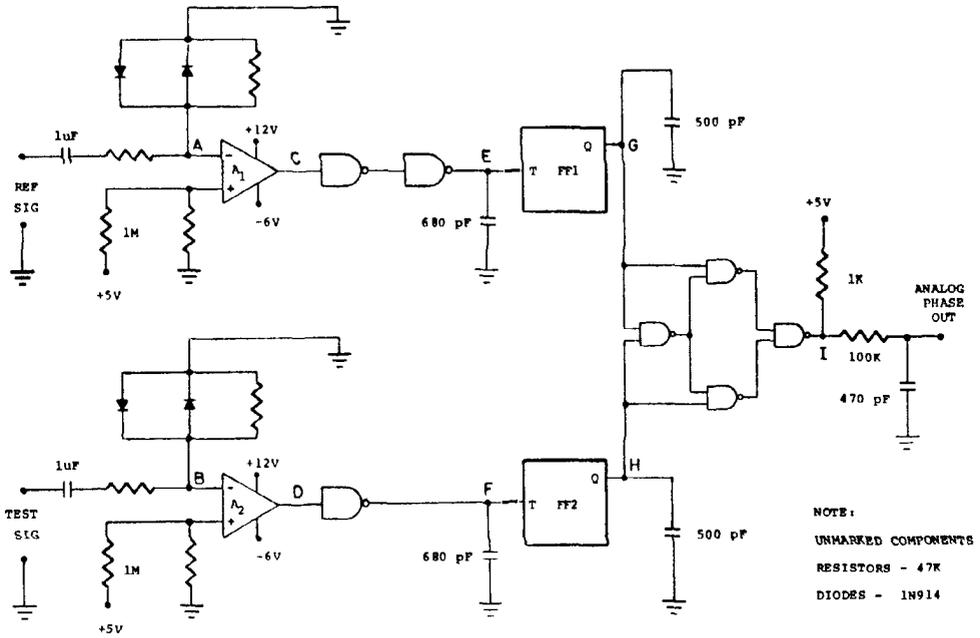
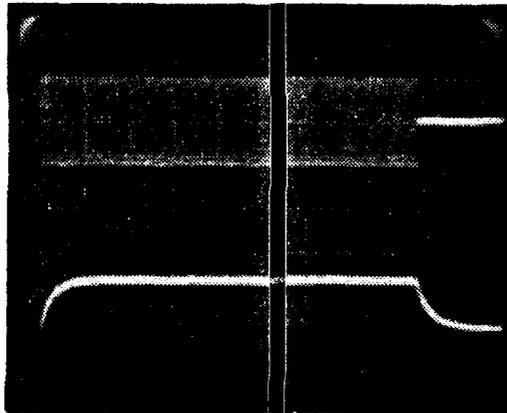


Figure 5. Phase detector circuit



Horizontal Scale: 0.2 ms/div Vertical Scale: 2 V/div

Figure 6. Phase detector response. Upper trace: Signal burst. Lower trace: Phase detector transient response

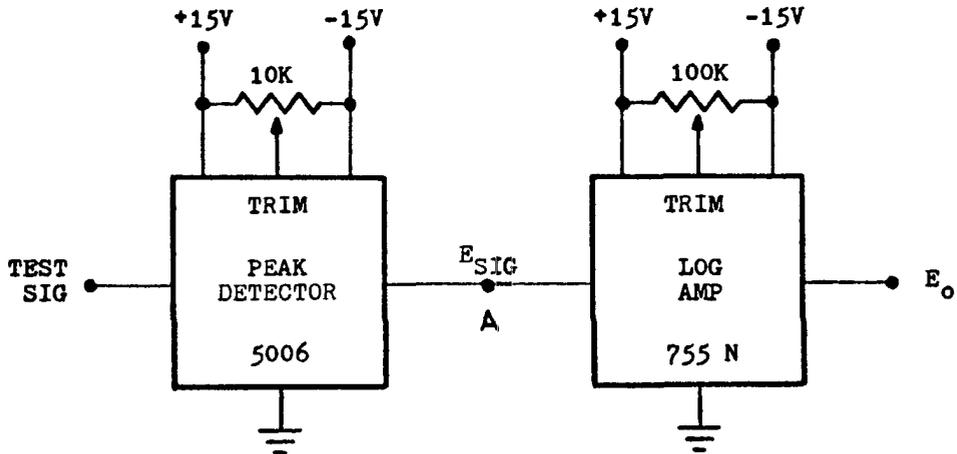


Figure 7. Amplitude detector circuit

The amplitude detector circuit (Fig.7) is a commercial peak detector (Optical Electronics 5006) driving a log amp providing dynamic range compression. The peak detector can measure peak-peak variations from - 33 dBV up to +17 dB within a 2% error. Only several microseconds are needed for transition times--well within requirements for the linear array system.

The microprocessor system is built around an Intel SBC 80/10(A) single board computer with a Burr-Brown 8616-A0 analog input-output board to provide the A/D conversion (within 44 μ secs) and memory loading as directed by the 80/10. The memory of the 80/10 is augmented by the SBC-064 RAM extension board with 64K bytes of memory. The SBC 80/10 is capable of addressing two of these memory boards over the Intel Multibus interface. A Tektronix development system was used to program a power-up sequence, a write operation where simulated data for a 128 x 128 array was successfully written into memory through the multiplexer and I/O board, and a read routine where data can be transferred from the electronic memory onto a digital cassette recorder. Other options for reading the data are also easily programmable (e.g., telephone modem, CRT display, line printer, etc.)

SUMMARY

The primary advantage of using microprocessor control of the data acquisition system is flexibility. Since the system is a testbed for research investigations in acoustic imaging, this flexibility is extremely important in being able to reconfigure the system to test new ideas. Similarly the capability of driving various peripheral devices with separate drive requirements is important. Both systems described in this paper have been designed and tested. The slower raster scan system is currently providing data for the study of various computer processing options in acoustic imaging. While our present research studies do not require the high speed data acquisition system its applicaiton is known and its feasibility has been demonstrated.

ACKNOWLEDGEMENTS

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